CLAIMS

What is claimed is:

1. A programmable pipeline processor for processing streaming input data, comprising:

an interface, for receiving field-delineated data from a field parser, the field parser connected to parse non-field delineated data from a streaming data source into the field-delineated data, under instructions from an external processing unit;

a field buffer that stores the field; and

at least one logic unit that performs at least one field operation on the field oriented data.

2. An apparatus as in claim 1 further comprising:

a programmable memory that receives, as an address, field oriented data from the field buffer, wherein the programmable memory serves as a substitution table for field data.

3. An apparatus as in claim 2 wherein

the substitution table contains alternate character equivalents for a set of character data.

4. An apparatus as in claim 2 wherein

the programmable memory includes multiple substitution tables that provide multiple character equivalents for a corresponding set of characters.

5. An apparatus as in claim 2 wherein

the substitution table is used to map uppercase letters to their lowercase equivalents for substitution.

6. An apparatus as in claim 1 further comprising:

at least two temporary registers for storing field oriented data from the field buffer, prior to use of the field oriented data by the logic unit.

7. An apparatus as in claim 6 wherein

a first data field is stored in a first temporary register from the field buffer;

a second data field is stored into a second temporary register; and

the logic unit is connected to compare a third data field from the field buffer with the first data field and a fourth data field from the field buffer with the second data field.

8. An apparatus as in claim 7 wherein

the logic circuit compares a third data field from the field buffer with the first data field and a fourth data field from the field buffer with the second field in two instructions.

9. An apparatus as in claim 6 wherein

a first data field is stored in a first temporary register from the field buffer;

a second data field is stored into a second temporary register; and

the logic unit is connected to compare a third data field from the field buffer with the first data field and with the second field.

10. An apparatus as in claim 9 wherein

the logic circuit compares a third data field from the field buffer with the first data field and a with the second field in a single instruction.

11. An apparatus as in claim 1 further comprising:

a data string register that stores data received from the external central processing unit to be used as an operand by the logic circuit.

12. An apparatus as in claim 11 wherein

at least one pointer specifies a location in the data string register to be used as the operand.

13. An apparatus as in claim 12 wherein

the logic circuit is connected to compare a data field from the field buffer with a data field from the data string register as specified by a first pointer.

14. An apparatus as in claim 13 wherein

the data field from the field buffer is simultaneously compared with a second data field from the data string register specified by a second pointer.

15. An apparatus as in claim 11 wherein

at least one logic unit performs a bit vector join operation using an operand from the data string register to determine the presence or absence of a particular field value in the field oriented data.

16. An apparatus as in claim 1 further comprising:

a data string register that stores data received from the external central processing unit to be used as an operand by the logic circuit; and

a temporary register for storing field oriented data from the field buffer, prior to use of the field oriented data by the logic unit; and

wherein an operand can originate from either the data string register or the temporary register.

17. An apparatus as in claim 1 wherein a field buffer location is reused when the streaming data source is paused.

18. An apparatus as in claim 1 further comprising:

a data string register that stores two or more operands received from the external central processing unit.

19. An apparatus as in claim 1 wherein the logic unit handles numeric data sign operations selected from the group consisting of floating point, integer and other numeric fields.

20. An apparatus as in claim 1 wherein the logic unit performs two or more filter operations in a single instruction.

21. A method for processing non-field delineated streaming data from a data source comprising:

receiving a non-field delineated data stream in a field buffer as an input data stream;

separating the input data stream into field oriented data under instruction from an external central processing unit;

sending field oriented data from the field buffer to at least one logic unit that performs at least one field operation on the field oriented data.